

Main Draw			
ARSC	QLD	[1] Sarbani MAITRA	
		A1 BYE	[1] Sarbani MAITRA
			11-2, 11-1, 11-1
GYM	QLD	[11] Ksenia ROBINSON	[1] Sarbani MAITRA
		5-11, 7-11, 10-12	[8] Jasmin DUMBLETON
CSGF	QLD	[8] Jasmin DUMBLETON	
			11-3, 11-2, 11-4 (12m)
SSCAU	QLD	[5] Paige WILSON	[1] Sarbani MAITRA
		A3 BYE	[5] Paige WILSON
			8-11, 8-11, 7-11 (13m)
SSCAU	QLD	[4] Lilly WILSON	[4] Lilly WILSON
		A4 BYE	[4] Lilly WILSON
			9-11, 9-11, 11-6, 11-8, 10-12 (39m)
SSC	QLD	[3] Orla CLARKE	[2] Joanne JOSEPH
		A5 BYE	[3] Orla CLARKE
			Walkover
		[6] Sarah HATTINGH	[6] Sarah HATTINGH
		11-4, 11-2, 11-7	[6] Sarah HATTINGH
ISC	QLD	[10] Kara NASH	
			2-11, 2-11, 3-11 (10m)
SSCAU	QLD	[9] Indigo-Rose LAWSON	[2] Joanne JOSEPH
		11-5, 10-12, 4-11, 11-3, 5-11	[7] Claudi BURGER
CSGF	QLD	[7] Claudi BURGER	
			3-11, 1-11, 3-11 (11m)
		BYE	[2] Joanne JOSEPH
		A8	[2] Joanne JOSEPH
MCCSC	VIC	[2] Joanne JOSEPH	

[4] Lilly WILSON

[4] Lilly WILSON

[6] Sarah HATTINGH

[8] Jasmin DUMBLETON

[5] Paige WILSON

10-12, 9-11, 11-8, 11-8, 11-7 (26m)

[5] Paige WILSON

BYE

C2

[7] **Claudi BURGER**

[7] Claudi BURGER

[8] Jasmin DUMBLETON

D1

BYE

[8] Jasmin DUMBLETON



BYE			
E1	[11] Ksenia ROBINSON		
[11] Ksenia ROBINSON			
	E5	[11] Ksenia ROBINSON	
BYE			
E2	BYE		
BYE			
		6-11, 11-8, 11-9, 8-11, 9-11 (27m)	[9] Indigo-Rose LAWSON
BYE			
E3	[10] Kara NASH		
[10] Kara NASH			
	2-11, 0-11, 2-11 (10m)	[9] Indigo-Rose LAWSON	
[9] Indigo-Rose LAWSON			
E4	[9] Indigo-Rose LAWSON		
BYE			

BYE	
F1	[10] Kara NASH
[10] Kara NASH	

The diagram illustrates a multi-processor system with a shared bus and a cache. The system components and their connections are as follows:

- Cache:** A rectangular block at the top, divided into two sections. The left section is labeled **BYE** and contains a box labeled **G1**. The right section is labeled **BYE** and contains a box labeled **G3**.
- Bus:** A horizontal line connecting the cache to the CPU.
- CPU:** A rectangular block at the bottom, divided into two sections. The left section is labeled **BYE** and contains a box labeled **G2**. The right section is labeled **BYE** and contains a box labeled **G3**.

The bus is a shared communication channel between the cache and the CPU. The cache and CPU are connected to the bus, and the bus is connected to the CPU. The cache and CPU are connected to the bus, and the bus is connected to the CPU.

BYE

H1

BYE

